RCA 1802 instruction set ordered by opcode

Opcode	Mnemonic	Instruction	Machine Cycles
00	IDL	Idle	2
01	LDN 1	Load D from address in register 1	2
02	LDN 2	Load D from address in register 2	2
03	LDN 3	Load D from address in register 3	2
04	LDN 4	Load D from address in register 4	2
05	LDN 5	Load D from address in register 5	2
06	LDN 6	Load D from address in register 6	2
07	LDN 7	Load D from address in register 7	2
08	LDN 8	Load D from address in register 8	2
09	LDN 9	Load D from address in register 9	2
0A	LDN A	Load D from address in register A	2
0B	LDN B	Load D from address in register B	2
0C	LDN C	Load D from address in register C	2
0D	LDN D	Load D from address in register D	2
0E	LDN E	Load D from address in register E	2
0F	LDN F	Load D from address in register F	2

Opcode	Mnemonic	Instruction	Machine Cycles
10	INC 0	Increment register 0	2
11	INC 1	Increment register 1	2
12	INC 2	Increment register 2	2
13	INC 3	Increment register 3	2
14	INC 4	Increment register 4	2
15	INC 5	Increment register 5	2
16	INC 6	Increment register 6	2
17	INC 7	Increment register 7	2
18	INC 8	Increment register 8	2
19	INC 9	Increment register 9	2
1A	INC A	Increment register A	2
1B	INC B	Increment register B	2
1C	INC C	Increment register C	2
1D	INC D	Increment register D	2
1E	INC E	Increment register E	2
1F	INC F	Increment register F	2
20	DEC 0	Decrement register 0	2
21	DEC 1	Decrement register 1	2

Opcode	Mnemonic	Instruction	Machine Cycles
22	DEC 2	Decrement register 2	2
23	DEC 3	Decrement register 3	2
24	DEC 4	Decrement register 4	2
25	DEC 5	Decrement register 5	2
26	DEC 6	Decrement register 6	2
27	DEC 7	Decrement register 7	2
28	DEC 8	Decrement register 8	2
29	DEC 9	Decrement register 9	2
2A	DEC A	Decrement register A	2
2B	DEC B	Decrement register B	2
2C	DEC C	Decrement register C	2
2D	DEC D	Decrement register D	2
2E	DEC E	Decrement register E	2
2F	DEC F	Decrement register F	2
30 aa	BR aa	Branch unconditionally	2
31 aa	BQ aa	Branch if Q is on	2
32 aa	BZ aa	Branch if zero	2
33 aa	BDF aa	Branch if DF is 1	2

Opcode	Mnemonic	Instruction	Machine Cycles
34 aa	B1 aa	Branch on external flag 1	2
35 aa	B2 aa	Branch on external flag 2	2
36 aa	B3 aa	Branch on external flag 3	2
37 aa	B4 aa	Branch on external flag 4	2
38	SKP	Skip 1 byte	2
39 aa	BNQ aa	Branch if Q is off	2
3A aa	BNZ aa	Branch if NOT zero	2
3B aa	BNF aa	Branch if DF is 0	2
3C aa	BN1 aa	Branch on NOT external flag 1	2
3D aa	BN2 aa	Branch on NOT external flag 2	2
3E aa	BN3 aa	Branch on NOT external flag 3	2
3F aa	BN4 aa	Branch on NOT external flag 4	2
40	LDA 0	Load D from address in register 0 and advance	2
41	LDA 1	Load D from address in register 1 and advance	2
42	LDA 2	Load D from address in register 2 and advance	2
43	LDA 3	Load D from address in register 3 and advance	2
44	LDA 4	Load D from address in register 4 and advance	2
45	LDA 5	Load D from address in register 5 and advance	2

Opcode	Mnemonic	Instruction	Machine Cycles
46	LDA 6	Load D from address in register 6 and advance	2
47	LDA 7	Load D from address in register 7 and advance	2
48	LDA 8	Load D from address in register 8 and advance	2
49	LDA 9	Load D from address in register 9 and advance	2
4A	LDA A	Load D from address in register A and advance	2
4B	LDA B	Load D from address in register B and advance	2
4C	LDA C	Load D from address in register C and advance	2
4D	LDA D	Load D from address in register D and advance	2
4E	LDA E	Load D from address in register E and advance	2
4F	LDA F	Load D from address in register F and advance	2
50	STR 0	Store D into memory pointed to by register 0	2
51	STR 1	Store D into memory pointed to by register 1	2
52	STR 2	Store D into memory pointed to by register 2	2
53	STR 3	Store D into memory pointed to by register 3	2
54	STR 4	Store D into memory pointed to by register 4	2
55	STR 5	Store D into memory pointed to by register 5	2
56	STR 6	Store D into memory pointed to by register 6	2
57	STR 7	Store D into memory pointed to by register 7	2

Opcode	Mnemonic	Instruction	Machine Cycles
58	STR 8	Store D into memory pointed to by register 8	2
59	STR 9	Store D into memory pointed to by register 9	2
5A	STR A	Store D into memory pointed to by register A	2
5B	STR B	Store D into memory pointed to by register B	2
5C	STR C	Store D into memory pointed to by register C	2
5D	STR D	Store D into memory pointed to by register D	2
5E	STR E	Store D into memory pointed to by register E	2
5F	STR F	Store D into memory pointed to by register F	2
60	IRX	Increment R(X)	2
61	OUT 1	Output from memory	2
62	OUT 2	Output from memory	2
63	OUT 3	Output from memory	2
64	OUT 4	Output from memory	2
65	OUT 5	Output from memory	2
66	OUT 6	Output from memory	2
67	OUT 7	Output from memory	2
68		*(Undefined for the RCA 1802)*	
69	INP 1	Input to memory and D	2

Opcode	Mnemonic	Instruction	Machine Cycles
6A	INP 2	Input to memory and D	2
6B	INP 3	Input to memory and D	2
6C	INP 4	Input to memory and D	2
6D	INP 5	Input to memory and D	2
6E	INP 6	Input to memory and D	2
6F	INP 7	Input to memory and D	2
70	RET	Return	2
71	DIS	Return and disable interrupts	2
72	LDXA	Load D via R(X) and advance	2
73	STXD	Store D via R(X) and decrement	2
74	ADC	Add with carry	2
75	SDB	Subtract D from memory with borrow	2
76	SHRC	Shift D right with carry	2
77	SMB	Subtract memory from D with borrow	2
78	SAV	Save T	2
79	MARK	Save X and P in T	2
7A	REQ	Reset Q	2
7B	SEQ	Set Q	2

Opcode	Mnemonic	Instruction	Machine Cycles
7C bb	ADCI bb	Add with carry immediate	2
7D bb	SBDI bb	Subtract D with borrow, immediate	2
7E	SHLC	Shift D left with carry	2
7F bb	SMBI bb	Subtract memory from D with borrow immediate	2
80	GLO 0	Get low byte of register 0	2
81	GLO 1	Get low byte of register 1	2
82	GLO 2	Get low byte of register 2	2
83	GLO 3	Get low byte of register 3	2
84	GLO 4	Get low byte of register 4	2
85	GLO 5	Get low byte of register 5	2
86	GLO 6	Get low byte of register 6	2
87	GLO 7	Get low byte of register 7	2
88	GLO 8	Get low byte of register 8	2
89	GLO 9	Get low byte of register 9	2
8A	GLO A	Get low byte of register A	2
8B	GLO B	Get low byte of register B	2
8C	GLO C	Get low byte of register C	2
8D	GLO D	Get low byte of register D	2

Opcode	Mnemonic	Instruction	Machine Cycles
8E	GLO E	Get low byte of register E	2
8F	GLO F	Get low byte of register F	2
90	GHI 0	Get high byte of register 0	2
91	GHI 1	Get high byte of register 1	2
92	GHI 2	Get high byte of register 2	2
93	GHI 3	Get high byte of register 3	2
94	GHI 4	Get high byte of register 4	2
95	GHI 5	Get high byte of register 5	2
96	GHI 6	Get high byte of register 6	2
97	GHI 7	Get high byte of register 7	2
98	GHI 8	Get high byte of register 8	2
99	GHI 9	Get high byte of register 9	2
9A	GHI A	Get high byte of register A	2
9B	GHI B	Get high byte of register B	2
9C	GHI C	Get high byte of register C	2
9D	GHI D	Get high byte of register D	2
9E	GHI E	Get high byte of register E	2
9F	GHI F	Get high byte of register F	2

Opcode	Mnemonic	Instruction	Machine Cycles
A0	PLO 0	Put D in low byte of register 0	2
A1	PLO 1	Put D in low byte of register 1	2
A2	PLO 2	Put D in low byte of register 2	2
A3	PLO 3	Put D in low byte of register 3	2
A4	PLO 4	Put D in low byte of register 4	2
A5	PLO 5	Put D in low byte of register 5	2
A6	PLO 6	Put D in low byte of register 6	2
A7	PLO 7	Put D in low byte of register 7	2
A8	PLO 8	Put D in low byte of register 8	2
A9	PLO 9	Put D in low byte of register 9	2
AA	PLO A	Put D in low byte of register A	2
AB	PLO B	Put D in low byte of register B	2
AC	PLO C	Put D in low byte of register C	2
AD	PLO D	Put D in low byte of register D	2
AE	PLO E	Put D in low byte of register E	2
AF	PLO F	Put D in low byte of register F	2
B0	PHI 0	Put D in high byte of register 0	2
B1	PHI 1	Put D in high byte of register 1	2

Opcode	Mnemonic	Instruction	Machine Cycles
B2	PHI 2	Put D in high byte of register 2	2
B3	PHI 3	Put D in high byte of register 3	2
B4	PHI 4	Put D in high byte of register 4	2
B5	PHI 5	Put D in high byte of register 5	2
B6	PHI 6	Put D in high byte of register 6	2
B7	PHI 7	Put D in high byte of register 7	2
B8	PHI 8	Put D in high byte of register 8	2
B9	PHI 9	Put D in high byte of register 9	2
BA	PHI A	Put D in high byte of register A	2
BB	PHI B	Put D in high byte of register B	2
BC	PHI C	Put D in high byte of register C	2
BD	PHI D	Put D in high byte of register D	2
BE	PHI E	Put D in high byte of register E	2
BF	PHI F	Put D in high byte of register F	2
C0 aa aa	LBR aa aa	Long branch unconditionally	3
C1 aa aa	LBQ aa aa	Long branch if Q is on	3
C2 aa aa	LBZ aa aa	Long branch if zero	3
C3 aa aa	LBDF aa aa	Long branch if DF is 1	3

Opcode	Mnemonic	Instruction	Machine Cycles
C4	NOP	No operation	3
C5	LSNQ	Long skip if Q is off	3
C6	LSNZ	Long skip if NOT zero	3
C7	LSNF	Long skip if DF is 0	3
C8	LSKP	Long skip	3
C9 aa aa	LBNQ aa aa	Long branch if Q is off	3
CA aa aa	LBNZ aa aa	Long branch if NOT zero	3
CB aa aa	LBNF aa aa	Long branch if DF is 0	3
CC	LSIE	Long skip if interrupts enabled	3
CD	LSQ	Long skip if Q is on	3
CE	LSZ	Long skip if zero	3
CF	LSDF	Long skip if DF is 1	3
D0	SEP 0	Set P from register 0	2
D1	SEP 1	Set P from register 1	2
D2	SEP 2	Set P from register 2	2
D3	SEP 3	Set P from register 3	2
D4	SEP 4	Set P from register 4	2
D5	SEP 5	Set P from register 5	2

Opcode	Mnemonic	Instruction	Machine Cycles
D6	SEP 6	Set P from register 6	2
D7	SEP 7	Set P from register 7	2
D8	SEP 8	Set P from register 8	2
D9	SEP 9	Set P from register 9	2
DA	SEP A	Set P from register A	2
DB	SEP B	Set P from register B	2
DC	SEP C	Set P from register C	2
DD	SEP D	Set P from register D	2
DE	SEP E	Set P from register E	2
DF	SEP F	Set P from register F	2
E0	SEX 0	Set X to point to register 0	2
E1	SEX 1	Set X to point to register 1	2
E2	SEX 2	Set X to point to register 2	2
E3	SEX 3	Set X to point to register 3	2
E4	SEX 4	Set X to point to register 4	2
E5	SEX 5	Set X to point to register 5	2
E6	SEX 6	Set X to point to register 6	2
E7	SEX 7	Set X to point to register 7	2

Opcode	Mnemonic	Instruction	Machine Cycles
E8	SEX 8	Set X to point to register 8	2
E9	SEX 9	Set X to point to register 9	2
EA	SEX A	Set X to point to register A	2
EB	SEX B	Set X to point to register B	2
EC	SEX C	Set X to point to register C	2
ED	SEX D	Set X to point to register D	2
EE	SEX E	Set X to point to register E	2
EF	SEX F	Set X to point to register F	2
F0	LDX	Load D via R(X)	2
F1	OR	Logical OR	2
F2	AND	Logical AND	2
F3	XOR	Exclusive OR	2
F4	ADD	Add	2
F5	SD	Subtract D from memory	2
F6	SHR	Shift D right	2
F7	SM	Subtract memory from D	2
F8 bb	LDI bb	Load D immediate	2
F9 bb	ORI bb	OR immediate	2

Opcode	Mnemonic	Instruction	Machine Cycles
FA bb	ANI bb	AND immediate	2
FB bb	XRI bb	Exclusive OR, immediate	
FC bb	ADI bb	Add immediate	2
FD bb	SDI bb	Subtract D from memory immediate byte	2
FE	SHL	Shift D left	2
FF bb	SMI bb	Subtract memory from D with borrow immediate byte	2

RCA 1802 instruction set ordered by mnemonic

Opcode	Mnemonic	Instruction	Machine Cycles
74	ADC	Add with carry	2
7C bb	ADCI bb	Add with carry immediate	2
F4	ADD	Add	2
FC bb	ADI bb	Add immediate	2
F2	AND	Logical AND	2
FA bb	ANI bb	AND immediate	2
34 aa	B1 aa	Branch on external flag 1	2
35 aa	B2 aa	Branch on external flag 2	2
36 aa	B3 aa	Branch on external flag 3	2
37 aa	B4 aa	Branch on external flag 4	2
33 aa	BDF aa	Branch if DF is 1	2
3C aa	BN1 aa	Branch on NOT external flag 1	2
3D aa	BN2 aa	Branch on NOT external flag 2	2
3E aa	BN3 aa	Branch on NOT external flag 3	2
3F aa	BN4 aa	Branch on NOT external flag 4	2
3B aa	BNF aa	Branch if DF is 0	2

Opcode	Mnemonic	Instruction	Machine Cycles
39 aa	BNQ aa	Branch if Q is off	2
3A aa	BNZ aa	Branch if NOT zero	2
31 aa	BQ aa	Branch if Q is on	2
30 aa	BR aa	Branch unconditionally	2
32 aa	BZ aa	Branch if zero	2
20	DEC 0	Decrement register 0	2
21	DEC 1	Decrement register 1	2
22	DEC 2	Decrement register 2	2
23	DEC 3	Decrement register 3	2
24	DEC 4	Decrement register 4	2
25	DEC 5	Decrement register 5	2
26	DEC 6	Decrement register 6	2
27	DEC 7	Decrement register 7	2
28	DEC 8	Decrement register 8	2
29	DEC 9	Decrement register 9	2
2A	DEC A	Decrement register A	2
2B	DEC B	Decrement register B	2
2C	DEC C	Decrement register C	2

Opcode	Mnemonic	Instruction	Machine Cycles
2D	DEC D	Decrement register D	2
2E	DEC E	Decrement register E	2
2F	DEC F	Decrement register F	2
71	DIS	Return and disable interrupts	2
90	GHI 0	Get high byte of register 0	2
91	GHI 1	Get high byte of register 1	2
92	GHI 2	Get high byte of register 2	2
93	GHI 3	Get high byte of register 3	2
94	GHI 4	Get high byte of register 4	2
95	GHI 5	Get high byte of register 5	2
96	GHI 6	Get high byte of register 6	2
97	GHI 7	Get high byte of register 7	2
98	GHI 8	Get high byte of register 8	2
99	GHI 9	Get high byte of register 9	2
9A	GHI A	Get high byte of register A	2
9B	GHI B	Get high byte of register B	2
9C	GHI C	Get high byte of register C	2
9D	GHI D	Get high byte of register D	2

Opcode	Mnemonic	Instruction	Machine Cycles
9E	GHI E	Get high byte of register E	2
9F	GHI F	Get high byte of register F	2
80	GLO 0	Get low byte of register 0	2
81	GLO 1	Get low byte of register 1	2
82	GLO 2	Get low byte of register 2	2
83	GLO 3	Get low byte of register 3	2
84	GLO 4	Get low byte of register 4	2
85	GLO 5	Get low byte of register 5	2
86	GLO 6	Get low byte of register 6	2
87	GLO 7	Get low byte of register 7	2
88	GLO 8	Get low byte of register 8	2
89	GLO 9	Get low byte of register 9	2
8A	GLO A	Get low byte of register A	2
8B	GLO B	Get low byte of register B	2
8C	GLO C	Get low byte of register C	2
8D	GLO D	Get low byte of register D	2
8E	GLO E	Get low byte of register E	2
8F	GLO F	Get low byte of register F	2

Opcode	Mnemonic	Instruction	Machine Cycles
00	IDL	Idle	2
10	INC 0	Increment register 0	2
11	INC 1	Increment register 1	2
12	INC 2	Increment register 2	2
13	INC 3	Increment register 3	2
14	INC 4	Increment register 4	2
15	INC 5	Increment register 5	2
16	INC 6	Increment register 6	2
17	INC 7	Increment register 7	2
18	INC 8	Increment register 8	2
19	INC 9	Increment register 9	2
1A	INC A	Increment register A	2
1B	INC B	Increment register B	2
1C	INC C	Increment register C	2
1D	INC D	Increment register D	2
1E	INC E	Increment register E	2
1F	INC F	Increment register F	2
69	INP 1	Input to memory and D	2

Opcode	Mnemonic	Instruction	Machine Cycles
6A	INP 2	Input to memory and D	2
6B	INP 3	Input to memory and D	2
6C	INP 4	Input to memory and D	2
6D	INP 5	Input to memory and D	2
6E	INP 6	Input to memory and D	2
6F	INP 7	Input to memory and D	2
60	IRX	Increment R(X)	2
C3 aa aa	LBDF aa aa	Long branch if DF is 1	3
CB aa aa	LBNF aa aa	Long branch if DF is 0	3
C9 aa aa	LBNQ aa aa	Long branch if Q is off	3
CA aa aa	LBNZ aa aa	Long branch if NOT zero	3
C1 aa aa	LBQ aa aa	Long branch if Q is on	3
C0 aa aa	LBR aa aa	Long branch unconditionally	3
C2 aa aa	LBZ aa aa	Long branch if zero	3
40	LDA 0	Load D from address in register 0 and advance	2
41	LDA 1	Load D from address in register 1 and advance	2
42	LDA 2	Load D from address in register 2 and advance	2
43	LDA 3	Load D from address in register 3 and advance	2

Opcode	Mnemonic	Instruction	Machine Cycles
44	LDA 4	Load D from address in register 4 and advance	2
45	LDA 5	Load D from address in register 5 and advance	2
46	LDA 6	Load D from address in register 6 and advance	2
47	LDA 7	Load D from address in register 7 and advance	2
48	LDA 8	Load D from address in register 8 and advance	2
49	LDA 9	Load D from address in register 9 and advance	2
4A	LDA A	Load D from address in register A and advance	2
4B	LDA B	Load D from address in register B and advance	2
4C	LDA C	Load D from address in register C and advance	2
4D	LDA D	Load D from address in register D and advance	2
4E	LDA E	Load D from address in register E and advance	2
4F	LDA F	Load D from address in register F and advance	2
F8 bb	LDI bb	Load D immediate	2
01	LDN 1	Load D from address in register 1	2
02	LDN 2	Load D from address in register 2	2
03	LDN 3	Load D from address in register 3	2
04	LDN 4	Load D from address in register 4	2
05	LDN 5	Load D from address in register 5	2

Opcode	Mnemonic	Instruction	Machine Cycles
06	LDN 6	Load D from address in register 6	2
07	LDN 7	Load D from address in register 7	2
08	LDN 8	Load D from address in register 8	2
09	LDN 9	Load D from address in register 9	2
0A	LDN A	Load D from address in register A	2
0B	LDN B	Load D from address in register B	2
0C	LDN C	Load D from address in register C	2
0D	LDN D	Load D from address in register D	2
0E	LDN E	Load D from address in register E	2
0F	LDN F	Load D from address in register F	2
F0	LDX	Load D via R(X)	2
72	LDXA	Load D via R(X) and advance	2
CF	LSDF	Long skip if DF is 1	3
CC	LSIE	Long skip if interrupts enabled	3
C8	LSKP	Long skip	3
C7	LSNF	Long skip if DF is 0	3
C5	LSNQ	Long skip if Q is off	3
C6	LSNZ	Long skip if NOT zero	3

Opcode	Mnemonic	Instruction	Machine Cycles
CD	LSQ	Long skip if Q is on	3
CE	LSZ	Long skip if zero	3
79	MARK	Save X and P in T	2
C4	NOP	No operation	3
F1	OR	Logical OR	2
F9 bb	ORI bb	OR immediate	2
61	OUT 1	Output from memory	2
62	OUT 2	Output from memory	2
63	OUT 3	Output from memory	2
64	OUT 4	Output from memory	2
65	OUT 5	Output from memory	2
66	OUT 6	Output from memory	2
67	OUT 7	Output from memory	2
B0	PHI 0	Put D in high byte of register 0	2
B1	PHI 1	Put D in high byte of register 1	2
B2	PHI 2	Put D in high byte of register 2	2
B3	PHI 3	Put D in high byte of register 3	2
B4	PHI 4	Put D in high byte of register 4	2

Opcode	Mnemonic	Instruction	Machine Cycles
B5	PHI 5	Put D in high byte of register 5	2
B6	PHI 6	Put D in high byte of register 6	2
B7	PHI 7	Put D in high byte of register 7	2
B8	PHI 8	Put D in high byte of register 8	2
B9	PHI 9	Put D in high byte of register 9	2
BA	PHI A	Put D in high byte of register A	2
BB	PHI B	Put D in high byte of register B	2
BC	PHI C	Put D in high byte of register C	2
BD	PHI D	Put D in high byte of register D	2
BE	PHI E	Put D in high byte of register E	2
BF	PHI F	Put D in high byte of register F	2
A0	PLO 0	Put D in low byte of register 0	2
A1	PLO 1	Put D in low byte of register 1	2
A2	PLO 2	Put D in low byte of register 2	2
A3	PLO 3	Put D in low byte of register 3	2
A4	PLO 4	Put D in low byte of register 4	2
A5	PLO 5	Put D in low byte of register 5	2
A6	PLO 6	Put D in low byte of register 6	2

Opcode	Mnemonic	Instruction	Machine Cycles
A7	PLO 7	Put D in low byte of register 7	2
A8	PLO 8	Put D in low byte of register 8	2
A9	PLO 9	Put D in low byte of register 9	2
AA	PLO A	Put D in low byte of register A	2
AB	PLO B	Put D in low byte of register B	2
AC	PLO C	Put D in low byte of register C	2
AD	PLO D	Put D in low byte of register D	2
AE	PLO E	Put D in low byte of register E	2
AF	PLO F	Put D in low byte of register F	2
7A	REQ	Reset Q	2
70	RET	Return	2
78	SAV	Save T	2
7D bb	SBDI bb	Subtract D with borrow, immediate	2
F5	SD	Subtract D from memory	2
75	SDB	Subtract D from memory with borrow	2
FD bb	SDI bb	Subtract D from memory immediate byte	2
D0	SEP 0	Set P from register 0	2
D1	SEP 1	Set P from register 1	2

Opcode	Mnemonic	Instruction	Machine Cycles
D2	SEP 2	Set P from register 2	2
D3	SEP 3	Set P from register 3	2
D4	SEP 4	Set P from register 4	2
D5	SEP 5	Set P from register 5	2
D6	SEP 6	Set P from register 6	2
D7	SEP 7	Set P from register 7	2
D8	SEP 8	Set P from register 8	2
D9	SEP 9	Set P from register 9	2
DA	SEP A	Set P from register A	2
DB	SEP B	Set P from register B	2
DC	SEP C	Set P from register C	2
DD	SEP D	Set P from register D	2
DE	SEP E	Set P from register E	2
DF	SEP F	Set P from register F	2
7B	SEQ	Set Q	2
E0	SEX 0	Set X to point to register 0	2
E1	SEX 1	Set X to point to register 1	2
E2	SEX 2	Set X to point to register 2	2

Opcode	Mnemonic	Instruction	Machine Cycles
E3	SEX 3	Set X to point to register 3	2
E4	SEX 4	Set X to point to register 4	2
E5	SEX 5	Set X to point to register 5	2
E6	SEX 6	Set X to point to register 6	2
E7	SEX 7	Set X to point to register 7	2
E8	SEX 8	Set X to point to register 8	2
E9	SEX 9	Set X to point to register 9	2
EA	SEX A	Set X to point to register A	2
EB	SEX B	Set X to point to register B	2
EC	SEX C	Set X to point to register C	2
ED	SEX D	Set X to point to register D	2
EE	SEX E	Set X to point to register E	2
EF	SEX F	Set X to point to register F	2
FE	SHL	Shift D left	2
7E	SHLC	Shift D left with carry	2
F6	SHR	Shift D right	2
76	SHRC	Shift D right with carry	2
38	SKP	Skip 1 byte	2

Opcode	Mnemonic	Instruction	Machine Cycles
F7	SM	Subtract memory from D	2
77	SMB	Subtract memory from D with borrow	2
7F bb	SMBI bb	Subtract memory from D with borrow immediate	2
FF bb	SMI bb	Subtract memory from D with borrow immediate byte	2
50	STR 0	Store D into memory pointed to by register 0	2
51	STR 1	Store D into memory pointed to by register 1	2
52	STR 2	Store D into memory pointed to by register 2	2
53	STR 3	Store D into memory pointed to by register 3	2
54	STR 4	Store D into memory pointed to by register 4	2
55	STR 5	Store D into memory pointed to by register 5	2
56	STR 6	Store D into memory pointed to by register 6	2
57	STR 7	Store D into memory pointed to by register 7	2
58	STR 8	Store D into memory pointed to by register 8	2
59	STR 9	Store D into memory pointed to by register 9	2
5A	STR A	Store D into memory pointed to by register A	2
5B	STR B	Store D into memory pointed to by register B	2
5C	STR C	Store D into memory pointed to by register C	2
5D	STR D	Store D into memory pointed to by register D	2

Opcode	Mnemonic	Instruction	Machine Cycles
5E	STR E	Store D into memory pointed to by register E	2
5F	STR F	Store D into memory pointed to by register F	2
73	STXD	Store D via R(X) and decrement	2
F3	XOR	Exclusive OR	2
FB bb	XRI bb	Exclusive OR, immediate	
68		*(Undefined for the RCA 1802)*	